WHAT IS CLAIMED IS:

1. A fractional-type phase-locked loop circuit for synthesising an output signal multiplying a frequency of a reference signal by a fractional conversion factor, the circuit including means for generating a modulation value, means for generating a feedback signal dividing the frequency of the output signal by a dividing ratio, the dividing ratio being modulated according to the modulation value for providing the conversion factor on the average, means for generating a control signal indicative of a phase difference between the reference signal and the feedback signal, means for controlling the frequency of the output signal according to the control signal, and means for compensating a phase error caused by the modulation of the dividing ratio, wherein

the means for compensating includes means for calculating an incremental value, indicative of an incremental phase error, according to the conversion factor and the modulation value, means for calculating a correction value accumulating the incremental value, and means for conditioning the control signal according to the correction value.

2. The circuit according to claim 1, wherein the means for generating the modulation value includes a sigma-delta modulator having an order at least equal to two.

3. The circuit according to claim 1, wherein the means for generating the modulation value includes a multi-bit modulator.

4. The circuit according to claim 1, wherein the means for generating the modulation value is responsive to an adjusting value consisting of an integer varying from zero to a pre-defined modulus, the means for calculating the incremental value including means for calculating a first value multiplying the modulation value by the pre-defined modulus and means for calculating a second value subtracting the first value from the adjusting value, and wherein the means for calculating the correction value includes means for accumulating the second value and means for scaling the accumulated second value according to the pre-defined modulus and the conversion factor.

5. The circuit according to claim 1, wherein the means for conditioning includes means for converting a representation of the correction value into a thermometric code consisting of a plurality of thermometric digits of even weight, and a plurality of digital-to-analog converters each one for a corresponding thermometric digit.

6. The circuit according to claim 5, wherein each thermometric digit consists of a thermometric bit, each digital-to-analog converter being a single-bit converter.

7. The circuit according to claim 6, wherein the correction value consists of a signed value, the digital-to-analog converters consisting of a first plurality of the single-bit converters each one for a corresponding thermometric bit representing a module of the correction value when positive and a second plurality of single-bit converters each one for a corresponding thermometric bit representing the module of the correction value when negative.

8. The circuit according to claim 5, wherein the means for conditioning further includes means for scrambling the thermometric digits.

9. The circuit according to claim 8, wherein the means for scrambling includes means for re-arranging the thermometric digits according to a random algorithm or a barrel shift algorithm.

10. In a fractional-type phase-locked loop circuit, a method of synthesising an output signal multiplying a frequency of a reference signal by a fractional conversion factor, the method including the steps of:

generating a modulation value,

generating a feedback signal dividing the frequency of the output signal by a dividing ratio, the dividing ratio being modulated according to the modulation value for providing the conversion factor on the average,

generating a control signal indicative of a phase difference between the reference signal and the feedback signal,

controlling the frequency of the output signal according to the control signal, and

compensating a phase error caused by the modulation of the dividing ratio,

characterised in that the step of compensating includes:

calculating an incremental value, indicative of an incremental phase error, according to the conversion factor and the modulation value,

calculating a correction value accumulating the incremental value, and

conditioning the control signal according to the correction value.

11. A circuit for compensating for a phase error between first and second signals, comprising:

a control circuit operable to receive a first data set, the control circuit further operable to produce a phase-error value from the first data set, the control circuit further operable to produce a second data set from the phase-error value; and

a generator coupled to the control circuit, the generator operable to generate a compensation signal corresponding to the second data set.

12. The circuit of claim 11 wherein the first data set comprises a modulation value operable to modulate a phase-locked-loop frequency divider.

13. The circuit of claim 11 wherein the control circuit comprises a first modifier operable to convert the first data set into a third data set.

14. The circuit of claim 13 wherein the control circuit further comprises a second modifier coupled to the first modifier, the second modifier operable to convert the third data set into the phase-error value.

15. The circuit of claim 14 wherein the control circuit further comprises a third modifier coupled to the second modifier, the third modifier operable to convert the phase-error value into the second data set.

16. The circuit of claim 11 wherein the generator comprises a first modifier operable to convert the second data set into a third data set.

17. The circuit of claim 16 wherein the generator further comprises a second modifier coupled to the first modifier, the second modifier operable to convert the third data set into a fourth data set.

18. The circuit of claim 17 wherein the generator further comprises a third modifier coupled to the second modifier, the third modifier operable to convert the fourth data set into the compensation signal.

19. A method of compensating for a phase error between first and second signals, comprising:

producing a phase-error value from a first data set;

producing a second data set from the phase-error value; and

generating a compensation signal corresponding to the second data set.

20. The method of claim 19 wherein the first data set comprises a modulation value operable to modulate a phase-locked-loop frequency divider.

21. The method of claim 19 wherein producing a phase-error value comprises:

convert the first data set into a third data set; and

converting the third data set into the phase-error value.

22. The method of claim 19 wherein generating a compensation signal comprises:

converting the second data set into a third data set;

converting the third data set into a fourth data set; and

converting the fourth data set into the compensation signal.

23. A phase-locked loop, comprising:

a circuit operable to introduce a phase error between first and second signals;

a control circuit operable to receive a first data set, the control circuit further operable to produce a phase-error value from the first data set, the control circuit further operable to produce a second data set from the phase-error value; and

a generator coupled to the control circuit, the generator operable to generate a compensation signal corresponding to the second data set.

24. An electronic system, comprising:

a circuit for compensating for a phase error between first and second signals, comprising:

a control circuit operable to receive a first data set, the control circuit further operable to produce a phase-error value from the first data set, the control circuit further operable to produce a second data set from the phase-error value; and

a generator coupled to the control circuit, the generator operable to generate a compensation signal corresponding to the second data set.